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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,778	03/06/2002	Robin Alexis Takasugi	10018457-1	8925

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EXAMINER	
CORRIELUS, JEAN M	

ART UNIT	PAPER NUMBER
2162	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,778	TAKASUGI ET AL.	
	Examiner	Art Unit	
	Jean M. Corrielus	2162	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/02/06.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,3-12,14-19,22,25 and 26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,3-12,14-19,22,25 and 26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on June 2, 2006, in which claims 1, 3-12, 14-19, 22, and 25-26 are presented for further examination.

Response to Arguments

2. Applicant's arguments with respect to the 112 1st paragraph in regard to claims 1, 3-12, 14-19 and 22 have been considered but are moot in view of the new ground(s) of rejection necessitated by amendment. However, Applicant's arguments with respect to the 112 2nd have been fully considered but they are not persuasive. (see examiner remark).

Remark

3. Applicant asserted that to the extent that the rejections are otherwise improper for lacking in legal basis. The examiner disagrees with the precedent assertion. It is not understood as what the applicant means by lacking in legal basis. The claims were under the basis established by patent laws, which is stated that claims 1-8 are rejected under 112 second as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites that "storing in a first register a value for tracking a number of data units that have been transferred into a buffer----". According to the specification page 6, lines 18-25, the register does not actually store any value for tracking the number of data units that have been transferred into a buffer, in fact the data mover 500 keeps track the progress of the transfer by managing the counter 502, which is decremented by the value of the block sector after each

successful block transfer from the host to the buffer. So after each unit of data transferred between the transfer system and the host, all the registers are updated. There is no indication showing the value of a register is modified based on a transfer of a data unit into a buffer nor a value storing in a second register to increment the value contained in the first register.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites that "storing in a first register a value for tracking a number of data units that have been transferred into a buffer----". According to the specification page 6, lines 18-25, the register does not actually store any value for tracking the number of data units that have been transferred into a buffer, in fact the data mover 500 keeps track the progress of the transfer by managing the counter 502, which is decremented by the value of the block sector after each successful block transfer from the host to the buffer. So after each unit of data transferred between the transfer system and the host, all the registers are updated. There is no indication showing the value of a register is modified based on a transfer of a data unit into a buffer nor a value storing in a second register to increment the value contained in the first register.

Claim 10 contains the deficiency as listed in the claim 1 above. Therefore, claim 10 is rejected using the same rationale as applied to claim 1 above.

Claim 19 contains the deficiency as listed in the claim 1 above. Therefore, claim 19 is rejected using the same rationale as applied to claim 1 above. In addition, claims 19 and 22 recite "a buffer's fullness". It is unclear to one having ordinary skill in the art as what applicant means by "buffer's fullness".

Claim 22 recites the limitation "the buffer's fullness" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed. In particular, the claimed feature of ***"transferring at least some of the data into the buffer responsive to the command"***; and the limitation as claimed in claim 1 are not described in the specification to enable one having ordinary skill in the art to make and use the invention. The specification paragraph [0022] defines the use of a data transfers between the data transfer buffer and the Host Interface or Storage Medium Interface are preferably in units of longwords As each longword is transferred the data Mover hardware decrements either the Host LW Ctr

513 or the SMI_LW_Ctr 514 depending on whether the transfer is to/from the host or the Storage Medium. In addition, the word counters internal to the Host Interface and Storage Medium Interface are decremented. At the end of a sector transfer to/from the Storage Medium 104, the Storage Medium Interface's internal word counter goes to 0, prompting it to send the sector acknowledgment SMI_SectXferred to the Data Mover, which is expecting this signal because its own SMI_LW_Ctr 514 has gone to 0. If there are more sectors to be transferred then upon receipt of the SMI_SectXferred 509 signal, the Data Mover 500 hardware reloads the SMI_LW_Ctr 514 from the register SMI_LW_PerSect 507 and issues another SMI_XferSect 508 signal to the Storage Medium Interface; and if there are more blocks to be transferred, then upon receipt of the Host_BlkXferred 404 signal, the Data Mover hardware reloads the Host_LW_Ctr 513 from the register Host_LW_PerBlk 506 and issues another Host_XferBlk 403 signal to the Host Interface 400.. However, such abovementioned of the specification does not provide form information to a client computer. Based on the analysis provided above and substantial evidence or reasoning, the examiner provided that one having ordinary skilled in the art would not recognize in the disclosure a description of the invention defined by the claims. The limitation as claimed in claim 1 ***"transferring at least some of the data into the buffer responsive to the command" is*** not supported by the as-filed disclosure, which is violated the written description requirement. In re Rasmussen, 650 F.2d 1212, 211 USPQ 323 (CCPA 1981). Applicant should duly note that the first paragraph of 35 U.S.C. 112 requires that the "specification shall contain a written description of the invention". Applicant should also note that the essential goal of the description of the invention requirement is to clearly convey the information that an applicant has invented the subject matter which is claimed; and to put the

public in possession of what the applicant claims as the invention." Furthermore, the written description requirement of the Patent Act promotes the progress of the useful arts by ensuring that patentees adequately describe their inventions in their patent specifications in exchange for the right to exclude others from practicing the invention for the duration of the patent's term. Indeed, the specification doe not satisfy the written description requirement because the specification does not describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1, 3-12, 14-19, 22, and 25-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter, specifically, as directed to an abstract idea.

While transferring data between a host device and a storage medium could be considered a tangible result, the body of claims 1, 3-12, 14-19, 22, and 25-26 do not appear to actually support the preamble by including a step or steps, which accomplish that act. Additionally, the claims 1, 3-12, 14-19, 22, and 25-26 appear to define non-statutory processes because they merely manipulate an abstract idea without a claimed limitation to a practical application. The language of the is not tied to an environment or machine which would result in a practical application that produce a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. claims 1, 3-12, 14-19, 22, and 25-26 recite a series of steps

without producing a concrete result. It does not appear to be anything subjective to raise an issue with whether theses steps produce a concrete result.

Claims 18 and 22 define non-statutory processes because they merely recite a software application not execute by a computer medium for transferring data between the host device and the storage medium. Such ASIC software application is not part of the host device for performing the act of transferring data. Claims 18 and 22 define an abstract idea without a claimed limitation to a practical application. The language of the is not tied to an environment or machine which would result in a practical application that produce a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. Applicant is advised to amend the claims by specifying the claim being directed to a practical application and producing a tangible result ***being executed*** by a general-purpose computer in order to correct the above indicated deficiencies.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Siegel US Patent no.5, 261,072.

As to claim 1, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to

execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "storing in a first register a value for tracking a number of data units that have been transferred into a buffer but that have not yet been transferred out the buffer" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "modifying the value contained in the first register in response to a transfer of a data unit out of the buffer" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "modifying a value contained in the first register in response to a transfer of a data unit into the buffer" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56).

As to claim 7, Siegel discloses the claimed "wherein the host device is a computer" (col.4, lines 37-50).

As to claim 8, Siegel discloses the claimed "wherein the storage medium comprises non-volatile semiconductor memory" (col.6, lines 15-62).

As to claim 9, Siegel discloses the claimed "implementing the method via an application specific integrated circuit (ASIC) (col.4, lines 1-9; col.7, lines 50-66).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3-6 and 10-12, 14-19, 22 and 25-26 as best understood by the examiner are rejected under 35 U.S.C. 103(a) as being unpatentable over Siegel US Patent no. 5,261,072 and Sefidvash US Patent no. 5,581,790.

As to claims 3- 6, 14-17 and 25-26, Siegel discloses the use of storing in the third register a value for incrementing a value contained in the first register" (col.7, lines 33-35); "storing in the register an address representing a location in the buffer where data is being transferred between the buffer and the host device" (col.8, lines 5-65): storing in the register an address representing a location in the buffer where data is being transferred between the buffer and storage medium (col.8, lines 5-65); storing in a sixth register an address representing a beginning of the buffer (col.8, lines 5-65); storing in the register an address representing and end of the buffer (col.8, lines 5-67) and storing in the register a value representing a storage capacity of the buffer (col.8, lines 5-65). However, Siegel does not explicitly disclose the use of second-eight registers. On the other hand, Sefidvash discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data. During the course of the data transfer, an integrity circuit 81 checks each word transferred for it parity value and also checks the entire block with an error detector

code to make sure the integrity of the data block transferred has been properly fulfilled and also keep track of the number of blocks which are properly transferred. Fig. 1A of Sefidvash discloses a multiple registers, wherein the register 34, register 36 and a counter feeder control unit keep track of the number of block of data that are being transferred. The system disclosed in Fig.6 of Sefidvash provided a method for measuring the number of bytes and number of blocks of data. Fig.2C uses the I/O buffer 36 of fig.1A to communicate to flag register 24, the interrupt register 34 and the mask register 36 in order to flag errors or to interrupt data transfer on a given protocol channel. These implications disclose the use of a second-eight register, wherein each one of the registers performs their own task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

As to claim 10, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "temporarily stores data that is transferred between the host device and the storage medium" (col.3, lines 40-50); "storing in a first register a value for tracking a number of data units that have been transferred into a buffer but that have not yet been transferred out the buffer" (col.6, lines 58-67;

since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "modifying the value contained in the first register in response to a transfer of a data unit out of the buffer" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "modifying a value contained in the first register in response to a transfer of a data unit into the buffer" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56). However, Siegel does not explicitly disclose the use of second-eight registers. On the other hand, Sefidvash discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data. During the course of the data transfer, an integrity circuit 81 checks each word transferred for it parity value and also checks the entire block with an error detector code to make sure the integrity of the data block transferred has been properly fulfilled and also keep track of the number of blocks which are properly transferred. Fig. 1A of Sefidvash discloses a multiple registers, wherein the register 34, register 36 and a counter feeder control unit keep track of the number of block of data that are being transferred. The system disclosed in Fig.6 of Sefidvash provided a method for measuring the number of bytes and number of blocks of data. Fig.2C uses the I/O buffer 36 of fig.1A to communicate to flag register 24, the interrupt register 34 and the mask register 36 in order to flag errors or to interrupt data transfer on a given protocol channel. These implications disclose the use of a second-eight register, wherein each one of the registers performs their own task. It would have been obvious

to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

As to claim 11, Siegel discloses the claimed "wherein the data transfer system is configured to modify the value contained in the first register in response to a transfer of a data unit between the buffer and the host device" (col.7, lines 33-65; col.8, lines 5-67).

As to claim 12, Siegel discloses the claimed "wherein the data transfer system is configured to modify the value contained in the first register in response to a transfer of a data unit between the buffer and the storage medium" (col.7, lines 33-65).

As to claim 18, Siegel discloses the claimed "implementing the method via an application specific integrated circuit (ASIC) (col.4, lines 1-9; col.7, lines 50-66).

As to claims 19, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "storing in a first register a value for determining a buffer's fullness" (col.6, lines 58-67; since register in general

used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "decrementing the value contained in the first register" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "incrementing the value contained in the first register" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56). However, Siegel does not explicitly disclose the use of second-eight registers. On the other hand, Sefidvash discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data. During the course of the data transfer, an integrity circuit 81 checks each word transferred for it parity value and also checks the entire block with an error detector code to make sure the integrity of the data block transferred has been properly fulfilled and also keep track of the number of blocks which are properly transferred. Fig. 1A of Sefidvash discloses a multiple registers, wherein the register 34, register 36 and a counter feeder control unit keep track of the number of block of data that are being transferred. The system disclosed in Fig.6 of Sefidvash provided a method for measuring the number of bytes and number of blocks of data. Fig.2C uses the I/O buffer 36 of fig.1A to communicate to flag register 24, the interrupt register 34 and the mask register 36 in order to flag errors or to interrupt data transfer on a given protocol channel. These implications disclose the use of a second-eight register, wherein each one of the registers performs their own special task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited

references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

As to claim 22, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "temporarily stores data that is transferred between the host device and the storage medium" (col.3, lines 40-50); "storing in a first register a value for determining a buffer's fullness" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "decrementing the value contained in the first register" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "incrementing the value contained in the first register" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56). However, Siegel does not explicitly disclose the use of second-eight registers. On the other hand, Sefidvash discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data. During the course of the data transfer, an

integrity circuit 81 checks each word transferred for it parity value and also checks the entire block with an error detector code to make sure the integrity of the data block transferred has been properly fulfilled and also keep track of the number of blocks which are properly transferred. Fig. 1A of Sefidvash discloses a multiple registers, wherein the register 34, register 36 and a counter feeder control unit keep track of the number of block of data that are being transferred. The system disclosed in Fig.6 of Sefidvash provided a method for measuring the number of bytes and number of blocks of data. Fig.2C uses the I/O buffer 36 of fig.1A to communicate to flag register 24, the interrupt register 34 and the mask register 36 in order to flag errors or to interrupt data transfer on a given protocol channel. These implications disclose the use of a second-eight register, wherein each one of the registers performs their own task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean M. Corrielus whose telephone number is (571) 272-4032. The examiner can normally be reached on 10 hours shift.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jean M Corrielus
Primary Examiner
Art Unit 2162

August 18, 2006